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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/410,974	10/01/1999	ANDREW M. JONES	99-TK-252	7705

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EXAMINER
PHILPOTT, JUSTIN M

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 11/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/410,974	JONES ET AL.	
	Examiner	Art Unit	
	Justin M Philpott	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133)
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/1/1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/1/1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: "8" (FIG. 1), "4I" and "4T" (FIG. 2), and "100" (FIG. 3). Furthermore, FIG. 2 includes a label located at the bottom of the INITIATOR box which appears to be "74", however, is unclearly written. Still further, the drawings do not include the following reference sign(s) mentioned in the description: "14" (page 6, line 18). A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

3. Claims 2 and 6 are objected to because of the following informality: "function" (line 2) must be changed to "functional" in order to remain consistent with the remainder of claims 2 and 6. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14 recites the limitations "primitive memory access operations" and "compound memory access operations" in claim 12. There is insufficient antecedent basis for these limitations in the claim. It appears claim 14 should be written to be dependent upon claim 13 and not claim 12. Applicant may overcome this rejection by amending claim 14 to be dependent upon claim 13.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3, 6, 7, 9, 12, 13, 16, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,397,325 to Jones et al.

Regarding claim 1, Jones teaches an integrated circuit (FIG. 1) comprising a plurality of functional modules (14) interconnected via a packet router (bus network 15), each functional

module (14) having packet handling circuitry (EVENT LOGIC) for generating and receiving packets conveyed by the packet router (15);

wherein at least a first set of the functional modules (14), acting as initiator modules, have packet handling circuitry (EVENT LOGIC) which includes request packet generation circuitry for generating request packets for implementing transactions (see abstract, lines 3-4), each request packet including a destination indicator (col. 3, line 38) identifying a destination of the packet and an operation field (i.e., opcode, see col. 6, lines 49-54) denoting the function to be implemented by the request packet, wherein the operation field comprises eight bits (i.e., 1 byte; byte 85 in FIG. 8) of which collectively denote the type of the packet (see col. 6, line 50; col. 7, lines 12-14; and col. 16, lines 17-19), denote the function (i.e., format, col. 6, line 52) to be implemented by the packet, and qualify the function (e.g., checks the length, col. 6, line 52).

While Jones does not specifically disclose exactly one, four, and three of these eight opcode bits corresponding to type, function, and qualifying, respectively, it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on Appellant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 2, Jones further teaches a second set ("at least one other module", col. 1, line 39) of the functional modules acting as target modules, each having packet handling circuitry ("circuitry", col. 15, line 56) which includes packet receiver logic (EVENT LOGIC, FIG. 1) for receiving the request packets and for generating respective response packets (col. 15, lines 55-62), wherein the packet type bit distinguishes between request packets and response packets (col. 16, lines 17-21).

Regarding claim 3, Jones teaches the function in request packets being a memory access operation (col. 15, lines 58-60).

Regarding claim 6, see the above regarding claim 1 and claim 2.

Regarding claim 7, see the above regarding claim 1 wherein Jones anticipates each functional module having packet handling circuitry.

Regarding claim 9, see the above regarding claim 1 and also see FIG. 18 wherein a port (30) connects the functional module (14) to a packet router (10).

Regarding claim 12, see the above regarding claim 1 and claim 2.

Regarding claim 13, see the above regarding claim 3.

Regarding claim 16, see the above regarding claim 3 and further see the table (col. 16, lines 5-15) indicating memory access operations which include load, store, and swap operations. Furthermore, the operation of read-modify-write is clearly anticipated by the previous-mentioned operations wherein load indicates read (col. 16, line 29), swap intuitively includes modify, and store indicates write (col. 16, lines 35-36).

Regarding claims 17 and 19, see the above regarding claim 3, and Jones further teaches the access memory operation includes cache operations (col. 17, lines 6-10).

8. Claims 4, 10, 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. in view of U.S. Patent No. 5,283,904 to Carson et al.

Regarding claims 4 and 14, Jones teaches the circuit according to claim 3 as discussed above, however, Jones does not specifically disclose one of the opcode bits distinguishing between primitive memory access operations involving a single request packet and compound memory access operations involving a plurality of request packets.

Carson teaches a programmable multi-processor interrupt controller (MPIC) system comprising a plurality of MPICs operating similar to the functional modules of Jones. Carson further teaches a physical mode (col. 5, line 60 – col. 6, line 6) wherein a unique 8-bit MPIC-ID (comparable to the 8-bit opcode of Jones) selects a single destination (i.e., primitive access) or a broadcast to all MPICs (i.e., compound access). Combining this teaching of Carson with the system of Jones would provide a more robust system, capable of initiating request packets for a plurality of modules or for just a single module determined by the opcode. Furthermore, one of ordinary skill in the art would advantageously implement such a system by utilizing a single bit of, for example, the operation family bits, of the opcode.

Regarding claim 10, see the above regarding claim 9 and claim 4.

Regarding claim 11, see the above regarding claim 10 and claim 2.

9. Claims 5, 8, 15, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. in view of U.S. Patent No. 5,704, 034 to Circello.

Regarding claims 5, 8 and 15, Jones teaches the circuit according to claims 1 and 2 as discussed above, however, Jones does not specifically disclose the request packets including a data object, the size of which is denoted by the operation qualifier.

Circello teaches a circuit for initializing a data processing system which involves sending signals (processor status PST and data signals DDATA) from a module (10, FIG. 1) to a system (7). The signals include a data object (DDATA) and the size of the data object is denoted by two bits of the PST (comparable to the operation qualifier of the opcode of Jones). Particularly, when a data object is transferred (indicated by bits 3:2 equalling 10, see FIG. 10), the size of the data object is denoted by bits 1:0 (wherein 00, 01, 10, and 11 denote in binary the number of bytes which are to be transferred). In the event transfers of more than four bytes were desired, at the time of the invention it would have been obvious to one of ordinary skill in the art to use additional bits in the operation qualifier (e.g., three) to denote the size of the data object (DDATA). Furthermore, applying the teachings of Circello with the system of Jones would provide an improved system wherein an element would advantageously be aware of the size of particular data transfers prior to transfer completion. Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the teachings of Circello with the system of Jones.

Regarding claims 18 and 20, Circello further teaches four PST bits denoting that the PST (e.g., operation field) is user defined (see FIG. 10, when PST[3:0] equals 0011).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 4,807,116 to Katzman et al. discloses a multiprocessor system comprising a plurality of processor modules interconnected by a bus for communications,

U.S. Patent No. 5,914,955 to Rostoker et al. discloses an integrated circuit comprising a network interface connected to a digital network employing a particular network protocol, and

European Patent No. EP0840221A1 to Jones and U.S. Patent No. 6,389,498 to Edwards et al. both disclose a microprocessor comprising the elements discussed above regarding Jones et al.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin M Philpott whose telephone number is 703.305.7357. The examiner can normally be reached on M-F, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D Vu can be reached on 703.308.6602. The fax phone numbers for the organization where this application or proceeding is assigned are 703.872.9314 for regular communications and 703.872.9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703.305.4750.

Justin M Philpott

November 1, 2002

HUY D. VU
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